

# Claims

- [c1] 1. A high resolution potentiometer comprising:  
a plurality of digital potentiometers connected in parallel.
- [c2] 2. A high resolution potentiometer comprising:  
a first digital potentiometer and a second digital potentiometer connected in parallel, wherein said first digital potentiometer is operable to be set to offer a first resistance and said second digital potentiometer is operable to be set to offer a second resistance, wherein said first resistance is not equal to said second resistance.
- [c3] 3. The high resolution potentiometer of claim 2, further comprising a control block to cause said first digital potentiometer and said second digital potentiometer to respectively offer said first resistance and said second resistance.
- [c4] 4. The high resolution potentiometer of claim 3, wherein said control block receives a desired resistance value and sets said first digital potentiometer to provide said first resistance and said second digital potentiometer to provide said second resistance such that the effective resis-

tance provided by said high resolution potentiometer at least substantially equals said desired resistance.

- [c5] 5. The high resolution potentiometer of claim 3, wherein said control block receives values corresponding to said first resistance and said second resistance, and sets said first digital potentiometer to provide said first resistance and said second digital potentiometer to provide said second resistance such that the effective resistance provided by said high resolution potentiometer at least substantially equals a desired resistance.
- [c6] 6. The high resolution potentiometer of claim 3, further comprising a resistor connected in series with said first digital potentiometer and said second digital potentiometer connected in parallel.
- [c7] 7. The high resolution potentiometer of claim 3, wherein said first potentiometer, said second potentiometer and said control block are implemented in a single integrated circuit.
- [c8] 8. A system comprising:  
a first digital potentiometer and a second digital potentiometer connected in parallel, wherein said first digital potentiometer is operable to be set to offer a first resistance and said second digital potentiometer is operable

to be set to offer a second resistance, wherein said first resistance is not equal to said second resistance.

- [c9] 9. The system of claim 7, further comprising:  
a control block to cause said first digital potentiometer and said second digital potentiometer to respectively offer said first resistance and said second resistance; and  
a processor.
- [c10] 10. The system of claim 9, wherein said control block receives a desired resistance value from said processor and sets said first digital potentiometer to provide said first resistance and said second digital potentiometer to provide said second resistance such that the effective resistance provided by said system at least substantially equals said desired resistance.
- [c11] 11. The system of claim 9, wherein said control block receives values corresponding to said first resistance and said second resistance from said processor, and sets said first digital potentiometer to provide said first resistance and said second digital potentiometer to provide said second resistance such that the effective resistance provided by said first digital potentiometer and said second digital potentiometer are connected in parallel at least substantially equals a desired resistance.

[c12] 12. The system of claim 9, further comprising a resistor connected in series with said first digital potentiometer and said second digital potentiometer connected in parallel.

[c13] 13. The system of claim 9, wherein said first potentiometer, said second potentiometer and said control block are implemented in the form of a single integrated circuit.